IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant	:	Jianhui Li	
Filed	:	01/03/2002	
TC/A.U.	:	2192	
Examiner	:	CHOW, CHIH-CHING	
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Customer No.	:	8791	

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

SUMMARY OF TELEPHONIC INTERVIEW

Sir:

A **Summary of Telephonic Interview** begins on page 2 of this paper.

SUMMARY OF TELEPHONIC INTERVIEW

Applicant thanks the Examiner for the courtesy of a telephonic interview on 03/07/2007. The following summary is to provide a complete and proper recordation of the substance of the interview:

(A) proposed amendments to claims 11 and 41 were shown as an exhibit as shown on the following two pages; no demonstration was conducted;

(B) claims 11 and 41 were discussed;

(C) no prior art was discussed;

(D) applicant proposed that claims 11 and 41 add --readable storage device-- following "processor" to overcome the Examiner's concerns about patentable subject matter with respect to the Office's Interim Guidelines; this amendment was suggested by Examiner Wei Zhen;

(E) applicant requested that the proposed amendment be entered by Examiner's amendment;

(F) no other pertinent matters were discussed;

(G) the Examiner asked that the proposed amendment by submitted by facsimile for the Examiner's consideration; and

(H) no part of the interview was conducted via electronic mail.

11. (currently amended):

An article of manufacture to translate a block of code from a source architecture that supports multiple-format registers to a target architecture that does not, the article of manufacture comprising a processor readable storage device including thereon sequences of instructions that, when executed, cause a computer processor to:

determine a register format of a source register operated on by a source instruction in a source block of code, the register format including an input instruction format and an output block format of the source block of code, the source block of code running in a source architecture, the source register having multiple formats and being used as an input of the source instruction, the input instruction format containing format of the source register expected by the source instruction, the output block format containing format of the source register after the source block of code is executed;

detect an instruction format inconsistency between the source register and a target register of a target architecture during a translation phase of a binary translation that translates the source block of code into a target block of code running in the target architecture;

emit a target instruction sequence corresponding to the source instruction into the target block of code;

emit a block inconsistency check code into prefix of the target block of code; and

emit a format update code to update a format register associated register format into the suffix of the target block of code.

41. (currently amended):

An article of manufacture to translate a block of code from a source architecture that supports multiple-format registers to a target architecture that does not, the article of manufacture comprising a processor readable storage device including thereon sequences of instructions that, when executed, cause a computer processor to:

determine a register format of a source register operated on by a source instruction in a source block of code, the register format including an input block format and an output block format of the source block of code, the source block of code running in a source architecture, the source register having multiple formats and a format register associated with the register format, the input block format containing format of the source register expected by the source block of code, the output block format containing format of the source register after the source block of code is executed;

detect a block format inconsistency between the source register and a target register of a target architecture during an execution phase of a binary translation that translates the source block of code into a target block of code running in the target architecture;

emit a target instruction sequence corresponding to the source instruction into the target block of code;

emit a block inconsistency check code into prefix of the target block of code; and

emit a format update code to update a format register associated register format into the suffix of the target block of code.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 03/07/2007

By /James Henry/

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